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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,450	04/19/2001	Satoshi Ishikura	60188-051	6764
7590 03/22/2004				
MCDERMOTT, WILL & EMERY 600 13th Street, N.W. Washington, DC 20005-3096		EXAMINER OWENS, DOUGLAS W		
		ART UNIT PAPER NUMBER		
		2811		
DATE MAILED: 03/22/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/837,450

Applicant(s)

ISHIKURA ET AL.

Examiner

Douglas W Owens

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3 and 5-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5-13, 16 and 17 is/are allowed.
- 6) ☒ Claim(s) 1-3, 14 and 15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.  
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

#### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 3, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 5,998,843 to Yoshida in view of page 45, Wolf, Silicon Processing for the VLSI Era, Volume 2 – Process Integration.

Regarding claim 1, Yoshida teaches a semiconductor device (Fig. 10, for example), comprising:

a source/drain (19) layer for a transistor; and

a dummy diffused layer (7);

an isolation structure formed between the source/drain diffused layer and the dummy diffused layer (5; between the PMOS and NMOS);

wherein, the source/drain layer has its surface silicided (26), and

wherein the dummy diffused layer has its surface covered with an anti-silicidation film (5), on which no gate electrode is provided.

Yoshida does not teach a shallow trench isolation between the source/drain diffused layer and the dummy diffused layer. Wolf teaches replacement of LOCOS

Art Unit: 2811

isolation in CMOS devices with shallow trench isolation. It would have been obvious to one of ordinary skill in the to incorporate the teaching of Wolf into the device taught by Yoshida, since it is desirable to prevent latchup.

Regarding claim 2, Yoshida teaches a semiconductor device, wherein the anti-silicidation film is an oxide film (Col. 4, lines 63 – 64).

Regarding claim 3, Yoshida teaches a semiconductor device, wherein a dopant, which has been introduced into the source/drain layer has not been introduced into the dummy diffused layer (different dopant types).

Regarding claim 14, Yoshida teaches a semiconductor device, wherein the dummy diffused layer is located between an analog circuit block and a digital circuit block.

Regarding claim 15, Yoshida teaches a semiconductor device, wherein, the dummy diffused layer is not electrically coupled to another component via an interconnect.

***Allowable Subject Matter***

4. Claims 5 – 13, 16 and 17 are allowed.

***Response to Arguments***

5. Applicant's arguments with respect to claims 1, 2, 3, 14 and 15 have been considered but are moot in view of the new ground(s) of rejection.


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DWO



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SUPERVISORY PATENT EXAMINER  
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